The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GILROY J. VANDENTOP and JUN-FEI ZHENG

Appeal No. 2006-1265
Application 10/020,911

ON BRIEF

Before THOMAS, JERRY SMITH, and MACDONALD, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appeal to the Board from the examiner's final rejection of claims 1 through 4, 14 through 16 and 31.

Independent claim 1 is reproduced below:

1. A method of fabricating an electro-optic semiconductor package, the method comprising:

providing an integrated circuit (IC) wafer having one or more IC contact pads, the IC contact pads being connected to an IC on the IC wafer;

providing an intermediate wafer having one or more intermediate contact pads, the intermediate contact pads being connected to an electro-optic arrangement on the intermediate wafer; and

direct copper bonding the C contact pads to adjacent intermediate contact pads, the electro-optic semiconductor package resulting.

The followings references are relied on by the examiner:

Fan et al., "Copper Wafer Bonding", Electrochemical and Solid State Letters, 2(10), (1999)pp. 534-536.

Appellants' admitted prior art at specification pages 1 through 3 in paragraphs [0003 -- 0005].

Claims 1 through 4, 14 through 16, and 31 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon the earlier - noted appellants' admitted prior art in view of Fan.

Rather than repeat the positions of the appellants and the examiner, reference is made to the Brief and Reply Brief for appellants' positions, and to the Answer for the examiner's positions.

OPINION

Generally, for the reasons set forth by the examiner in the answer, as expanded upon here, we sustain the rejection of all claims on appeal under 35 U.S.C. § 103. At the outset, we note that appellants only present arguments as to independent claim 1 and dependent claim 31. In the absence of any arguments as to any other dependent claim on appeal in the brief, we sustain the rejection of all of them.

Initially, we reproduce paragraph [0005] at specification pages 2 and 3 as filed:

> While the above-described conventional approach has been satisfactory in some circumstances, certain difficulties remain. One particular difficulty related to the placement of the optical detector on the IC wafer. Specifically, it has been determined that C4 bonding results in a "gap" between the wafers, and that the gap can lead to a number of problems from an optical standpoint. For example, aligning the optical arrangement with the photodetector requires a significant amount of precision in order to adequately couple the optical energy across the interface between the two wafers. Furthermore, the indirect bonding approach results in gaps on the order of 60 microns that can allow optical energy to escape regardless of how well the wafers are aligned. While the above-described optical losses could be avoided to some degree by placing the optical detector on the intermediate wafer, it has been determined that C4 bonding can also present problems from an electrical standpoint. For example, unwanted interconnect delay, resistance, capacitance, and loop inductance can all result from the C4 balls that are disposed between the IC contact pads and the intermediate contact pads. Thus,

> manufacturers and designers of conventional electro-optic semiconductor packages are faced with the difficult choice between the optical losses associated with IC wafer placement of the optical detector and the electrical losses associated with intermediate wafer placement of the optical detector.

As appellants' specification indicates in specification paragraph [0004] (not reproduced above) as well as in the portion reproduced in the last paragraph, it was common in the art to place an optical detector on the IC wafer. It appears that the prior art recognizes, according to the teachings at the top of specification page 3 as we reproduced above, that it was known that optical losses could be avoided to some degree by placing the optical detector on the intermediate wafer. On the other hand, doing so would have presented problems of an electrical nature rather than of an optical nature. Listed electrical problems are interconnect delays, resistance, capacitance and certain inductances result from the use of the so-called C4 ball approach of the prior art if this mechanism is used to affix or otherwise contact the IC contact pads of the IC wafer with the corresponding contact pads of the intermediate wafer. Therefore, the assessment of the prior art here clearly indicates that the

inter-connectability of the respective contact pads of an intermediate wafer and IC processor wafer presents an electrical rather than an optical problem.

Appellants have not contested and it is abundantly clear to us that the examiner's view is correct at page 3 of the answer that appellants' admitted prior art teaches substantially all of the subject matter of independent claim 1 on appeal, except for the feature of utilizing direct copper bonding as the mechanism to affix the respective contact pads of the adjacent intermediate wafer and the semiconductor wafer as claimed.

As to the basic teachings of Fan, the examiner considered the use of direct copper bonding to have been an obvious solution to the known problems in the art. With this general assessment of the examiner we strongly agree. As the examiner notes in his analysis, the use of direct bonding of copper to copper as taught by Fan has significant electrical advantages to eliminate known prior art disadvantages utilizing the solder ball or so-called C4 approach. Direct copper bonding allows resulting connections to have low electrical resistivity and high electromigration resistance such as to reduce interconnect RC delays between integrated circuits as expressed in the initial paragraph at column 1 in the text of the Fan article at page 534.

Therefore, it may be fairly stated that the known problems with prior art approaches as set forth in the quoted portions from the specification reproduced earlier in this opinion were clearly solvable by the use of direct copper bonding as outlined by Fan. It is interesting to note that the Fan article was utilized by appellants as an exemplary methodology to actually perform direct copper bonding as explained in specification paragraph [0020] and as illustrated in the details of element 56 in figure 4 of the disclosed invention.

Appellants' arguments in the brief and reply brief appear to recognize that Fan teaches the advantages of using direct copper bonding to connect electrical devices, such as the remarks made at the middle of page 5 of the principal brief on appeal. We do not agree with appellants' continued observation there that Fan fails to suggest similar advantages might be obtained by using direct copper bonding with optical devices. This misstates the issue. Nor do we agree with the appellants' observation at page 6 of the principal brief on appeal regarding the fabrication of optical devices since the claims do not recite that optical devices per se are actually fabricated. Clearly, the admitted prior art recognizes that they have already been fabricated and placed upon an intermediate wafer.

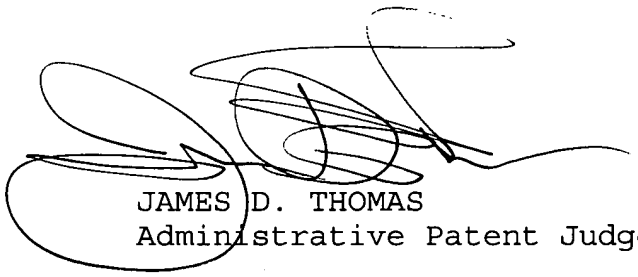
Furthermore, appellants' remarks at pages 2 and 3 of the reply brief give an incomplete understanding as what they have admitted to be in the prior art of their own disclosure. As the examiner attempts to reason through in the answer, the teaching value of Fan clearly applies to any and all types of integrated circuit devices on wafers with no particular distinction made to any type of device per se. On the other hand, while Fan may be fairly stated to not explicitly disclose to use direct copper bonding with intermediate wafers having electro-optical devices thereon, Fan does clearly teach that it was known in the art to solve known electrical connectivity problems by connecting all types of electrical devices on separate integrated circuit wafers by direct copper bonding.

As to dependent claim 31, we note initially that no arguments are presented as to this claim in the reply brief. Claims 31 recites that the direct copper bonding enables optical losses of the completed package to be minimized. This recitation is the functional result or property of the combined package and not a further recitation of any process step per se of the claimed methodology of parent independent claim 1. In the

context of appellants' admitted prior art, that is, in the paragraph we reproduced earlier in this opinion, prior art approaches of not placing the optical detector on the intermediate wafer chip with the optical devices but rather placing it on the integrated circuit wafer presented alignment problems and gaps between the wafers when the prior art connectivity approaches were followed such as to allow optical energies to be communicated across an interface from one wafer to another or to otherwise escape. The noted paragraph we reproduced earlier appears to recognize as well that optical losses would be avoided at least to some degree by the placing of the optical detector per se on the intermediate wafer rather than to continuing to use the approach followed in the prior art of placing it on the IC chip wafer. Fan solves the electrical problems.

In view of the foregoing, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).



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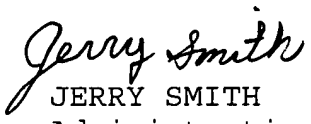
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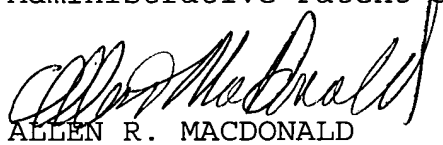
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